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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/028,276	Applicant(s) ATSUMI, SHIGERU	
	Examiner Jesse A Fenty	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *30 September 1999* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,13,14 and 21-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13,14 and 21-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) ☐ Notice of References Cited (PTO-892)
15) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2 and 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu et al. (U.S. Patent No. 4,471,373).

In re claim 1 and 21-26, Shimizu (Figs. 1-3, 18) discloses a semiconductor integrated circuit device comprising a semiconductor substrate (10) on which a plurality of transistors (Q1, Q2, QE1, QE2, QE3) including gate insulation films of different thicknesses are formed; an input/output terminal (5) formed on the substrate, wherein a transistor (QE2) physically connected directly to the input/output terminal being one of the transistors other than a transistor having the thinnest gate insulation film.

In re claim 2, Shimizu discloses the device of claim 1, further comprising a power supply terminal (5), a transistor (QE3) connected directly to the power supply terminal

being one of the transistors other than the transistor having the thinnest gate insulation film.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-9, 13-14 and 27-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (U.S. Patent No. 4,471,373).

In re claims 3-9, 13-14 and 27-42, Shimizu (Figs. 1-3, 18) discloses the devices of claims 1 and 24 respectively, including a memory array (2), a decoder portion (3), an input/output circuit (4), and enhancement type MIS transistors having a high breakdown voltage structure, i.e. a thick gate oxide film, and terminals for external connections (5) (column 1, lines 63-68; column 2, lines 23-63). Shimizu discloses the use of thin gate oxide transistors for the 'read' operation of an EPROM device and thick gate oxide transistors used for the 'write' operation, as well as other peripheral circuits (column 2, lines 45-51 Shimizu does not expressly disclose a ground terminal connected to the power supply terminal, a regulator circuit or a level shifter circuit of which one of the transistors receiving a lower level signal is a transistor having the thinnest gate insulation film. However, it would have been obvious to one skilled in the art at the time of the invention to couple a power supply line to a respective ground line. With the use of thin gate oxide transistors and lower voltages in the memory array and thick gate oxide transistors with higher voltages for peripheral circuits with a decoder circuit in between, it would have been obvious to one skilled in the art at the time of the invention to construct other in between circuits for the purpose of creating a buffer between the low and high voltage regions of the circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on M-F 9-5.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JAF
December 2, 1999

Mahshid Saadat

Mahshid Saadat
Supervisory Patent Examiner
Technology Center 2800